

REMARKS

Claims 1-68 are currently pending with claims 3-5, 8-11, 17-37, 39-45, and 47-63 being withdrawn and claims 1, 2 and 64 being independent. The specification has been amended to correct minor typographical errors. No new matter has been introduced.

Applicant acknowledges with appreciation the GRANT of the Petitions to Revive filed on December 18, 2003, and July 20, 2004.

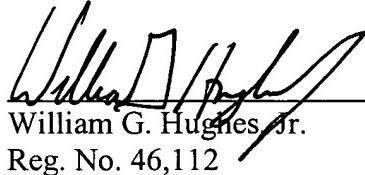
Further, Applicant thanks the Examiner for the courtesies extended during the telephone conversation of January 4, 2005. At the Examiner's request, Applicant submits herewith a copy of Applicant's response that was filed on July 13, 2003.

Therefore, and in accordance with the above-referenced telephone conversation, Applicant requests that the Examiner issue a new Advisory Action or Office Action, advising Applicant of the status of the present application and claims, including any relevant deadline(s) for response.

In the event that the Examiner feels it would be helpful, the Examiner is invited to contact the undersigned Attorney.

No fee is believed to be due in connection with this paper. In the event that any fees are due, please apply any charges or credits to deposit account 06-1050.

Respectfully submitted,



\_\_\_\_\_  
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Date: January 7, 2005

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Yamazaki, et al. Art Unit : 2813  
Serial No. : 09/898,986 Examiner : Laura Schillinger  
Filed : July 3, 2001  
Title : SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING  
THE SAME

**MAIL STOP AF**  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

# APPENDIX

## (Reply to Action)



## THE UNITED STATES PATENT AND TRADEMARK OFFICE

**COPY**

Applicant : Yamazaki, et al.

Art Unit : 2813

Serial No. : 09/898,986

Examiner : Laura Schillinger

Filed : July 3, 2001

Title : SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE  
SAME**MAIL STOP AF**

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

**REPLY**

In reply to the action mailed March 13, 2003, please amend the application as indicated on the following pages. Applicant asks that all claims be allowed in view of the amendment to the claims and remarks contained on the following sheets, a total of 11 pages.

Enclosed is a \$110.00 check for the One Month Extension of Time fee. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

Date: July 11, 2003  
\_\_\_\_\_  
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In the claims:

**Please amend the claims as follows:**

Claim 1. (Previously Amended) A method of manufacturing a semiconductor device, comprising the steps of:

forming first and second semiconductor islands on an insulating surface;

introducing ions of a p-type impurity into at least a portion of only said first semiconductor island without mass separation wherein said portion is to become a channel region of a thin film transistor; and

subjecting said first and second semiconductor islands to a thermal oxidization process to form a thermal oxide film on the first and second semiconductor islands wherein said p-type impurity is incorporated into the thermal oxide film formed on said first semiconductor island;

wherein a concentration of said p-type impurity monotonically decreases from a first portion distant from an upper surface of the first semiconductor island to a second portion close to the upper surface in a depthwise direction of the first semiconductor island.

Claim 2. (Previously Amended) A method of manufacturing a semiconductor device as claimed in claim 1,

wherein said first semiconductor island constitutes a p-channel semiconductor device;

wherein said second semiconductor island constitutes an n-channel semiconductor device; and

wherein said p-channel semiconductor device and said n-channel semiconductor device are complementarily combined with each other to form a CMOS structure.

Claims 3-5. (Withdrawn)

Claim 6. (Previously Amended) A method of manufacturing a semiconductor device as claimed in claim 1, wherein a thickness of said first semiconductor island is 100 to 1000Å.

Claim 7. (Previously Amended) A method of manufacturing a semiconductor device as claimed in claim 2, wherein a thickness of said first semiconductor island is 100 to 1000Å.

Claims 8-11. (Withdrawn).

Claim 12. (Original) The method according to claim 1 wherein said semiconductor device is a liquid crystal display device.

Claim 13. (Original) The method according to claim 1 wherein said semiconductor device is an electroluminescent display device.

Claim 14. (Original) The method according to claim 1 wherein said semiconductor device is a video camera.

Claim 15. (Original) The method according to claim 1 wherein said semiconductor device is a personal computer.

Claim 16. (Original) The method according to claim 1 wherein said semiconductor is a projection system.

Claims 17-37. (Withdrawn).

Claim 38. (Previously Added) The method according to claim 1 further comprising a step of forming a gate electrode over said first semiconductor island with said thermal oxide film interposed therebetween as a gate insulating film wherein said gate insulating film contains boron at a concentration of  $1 \times 10^{17}$  to  $1 \times 10^{20}/\text{cm}^3$ .

Claims 39-45. (Withdrawn).

Claim 46. (Previously Added) The method according to claim 1 wherein said p-type impurity is boron.

Claims 47-63. (Withdrawn).

Claim 64. (New) A method of manufacturing a semiconductor device comprising:  
    forming a layer of a crystalline semiconductor film on a surface of a substrate,  
    where the layer includes a portion to be used as a channel region of a thin film transistor;  
    introducing ions of a p-type impurity into the portion;  
    selecting a temperature corresponding to a mobility of the ions with respect to an  
    interface between the crystalline semiconductor film and an oxide;  
    subjecting the layer to a thermal oxidation process at the temperature to form a  
    thermal oxide on the layer into which a portion of the ions diffuse from the crystalline  
    semiconductor film, such that a desired concentration gradient of the ions within the crystalline  
    semiconductor film is obtained that provides a corresponding adjustment to a threshold voltage  
    of the thin film transistor.

Claim 65. (New) The method of claim 64 in which the desired concentration gradient  
concentration of the ions monotonically decreases from a first portion distant from an upper  
surface of the crystalline semiconductor film to a second portion close to the upper surface in a  
depthwise direction of the crystalline semiconductor film.

Claim 66. (New) The method of claim 64 in which introducing ions of the p-type  
impurity comprises performing ion implantation of the ions.

Claim 67. (New) The method of claim 64 in which introducing ions of the p-type  
impurity comprises performing a plasma doping of the ions without mass separation.

Claim 68. (New) The method of claim 64, in which selecting the temperature comprises  
selecting a temperature in the range of approximately 800°C to 1000°C.

## REMARKS

Claims 1-68 are pending. Claims 3-5, 8-11, 17-37, 39-45, and 47-63 are withdrawn from consideration. In particular, claims 32-37, 39-45, and 47-63, which were submitted in the Reply filed November 14, 2002, are withdrawn in the pending Office Action by virtue of a constructive election.

Claims 64-68 are added by virtue of this amendment. Applicant submits that claims 64-68 should not be subject to withdrawal, since, for example, they are directed to the same species as claim 1 (for example, dependent claim 65 recites the limitation of "a p-type impurity region which monotonically decreases").

Regarding preliminary matters, Applicant thanks the Examiner for acknowledging Applicant's claim for foreign priority under 35 U.S.C. 119, in the Office Action dated August 14, 2003. However, Applicant notes that the Examiner has not acknowledged Applicant's claim for domestic priority under 35 U.S.C. 120, and requests such acknowledgement from the Examiner in the next official communication.

Further, Applicant notes that the Examiner has not indicated acceptance of the drawings filed in the present application, and requests such an indication from the Examiner in the next official communication.

Applicant further thanks the Examiner for consideration of the reference listed on the Form PTO-1449 that was submitted with the IDS submitted on November 14, 2002.

However, Applicant notes that an IDS was provided with the filing of the present application (on July 3, 2001) that the Examiner has not yet acknowledged, and Applicant respectfully requests such acknowledgement from the Examiner in the next official communication.

More specifically, the July 3 IDS lists, on Forms PTO-1449 and Forms PTO-892 (four sheets total) all of the references that are of record in the parent application(s) of the present application (as indicated in the transmittal papers associated with the filing of the present application). The August 14 Office Action includes these listings marked "not considered," and states that the reference listings were ..." improper and will not be considered as an IDS," and that "...date of any re-submission...will be the date of submission for purposes of determining

compliance with the requirements" (see August 14 Office Action, page 2, paragraph 2). The Office Action further requests copies of a number of non-patent references listed in the IDS.

Applicant respectfully believes these actions to be improper on a number of fronts. First, Applicant points out that, as mentioned above, the references in question are references previously cited in parent application(s). Therefore, the Examiner of an application is under a duty to consider such references, regardless of whether they are submitted in the present application (See, e.g., MPEP 609(I)(A)(2), stating, "(t)he Examiner *will consider* information which has been considered by the Office in a parent application when examining...a divisional application filed under 37 CFR 1.53(b)," emphasis added). Further, the same MPEP section goes on to point out that "(s)uch information need not be resubmitted in the continuing application unless the applicant desires the information to be printed on the patent" (*Id.*).

Second, Applicant respectfully submits that the date of submission of the IDS is properly considered to be its filing date, i.e., July 3, 2001. That is, the Office Action errs in stating that the IDS fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP 609. Those provisions deal with substantive issues of proper identification and timely submission of references, not formal matters of how those references are listed when submitted.

For example, the August 14 Office Action refers to MPEP 609(III)(C)(1), which identifies "noncomplying" Information Disclosure Statements, such as non-compliance with timing requirements or requirements for appropriate fees and/or statements. This section does not address matters of form. In contrast, MPEP 609(III)(C)(2) states that "If...citations are submitted on a list other than on a Form PTO-1449...the Examiner may write 'all considered' and his or her initials to indicate that all citations have been considered."

Third, regarding the foreign-language references, Applicant submits that, under 37 CFR 1.98(d), there is no requirement to submit copies of these references, inasmuch as they were already properly submitted in the parent applications (specifically, Application No. 08/890,591, filed July 8, 1997, and Application No. 09/272,701, filed March 18, 1999). Nonetheless, if these copies were somehow misplaced from the parent file, Applicant would be happy to obtain and provide additional copies for the Examiner's convenience.

In concluding remarks regarding the IDS submitted on July 3, 2001, Applicant is happy to provide, for the Examiner's convenience, a listing of the references in question on a clean

Form PTO-1449 submitted with the present Reply. However, inasmuch as this listing is merely a re-statement of previously-submitted references, all of which are believed to be of record in the parent application(s), Applicant respectfully submits that no additional statement or fee is due at this time. Applicant requests that the Examiner indicate acknowledgement of submission and consideration of the listed references by including an initialed copy of the clean Form PTO-1449 submitted with this Reply when transmitting the next official communication, so that the references may be properly listed on the face of any patent that may issue from the present application.

Regarding the constructive election of claims 32-37, 39-45, and 47-63 (which were submitted in the Reply filed November 14, 2002) that is dictated by the withdrawal of these claims in the pending Office Action, Applicant respectfully submits that claims 55-63 appear to have been incorrectly or inadvertently included in the list of withdrawn claims.

Specifically, the Office Action states that claims 32-37 are withdrawn as being dependent from non-elected claim 11, whereas claims 39-45 and 47-53 are said to constitute a separate species from that of elected claim 1, for the reason that "they do not require a p-type impurity region which monotonically decreases (see Office Action, page 2, paragraph 1). First, Applicant notes that claim 54 depends from withdrawn claim 48, and so apparently should have been included in the listing of claims 47-53.

Second, no mention of claims 55-63 is made during the discussion of claims to be withdrawn. Nonetheless, these claims are later included in the listing of withdrawn claims (see Office Action, page 1, paragraph 2). In reading claim 55, Applicant notes that the primary difference between amended claim 1 and claim 55 is the recitation of "plasma doping," and that claim 55 does include the limitation of a monotonically decreasing p-type impurity, as recited therein. Therefore, Applicant respectfully submits that claim 55 should not have been withdrawn from consideration, and requests examination on the merits in the Examiner's next official communication.

Claims 1, 2, 6, 7, 12-16, 38, and 46 are rejected under 35 U.S.C. 112(1), as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to make and/or use the invention.

Regarding this rejection, the Office Action points out that each of these claims recite the terminology “without mass separation,” and cites this claim element(s) as the basis for the rejection. Specifically, the Office Action states that “...there is no disclosure within the specification of how Applicant’s method prevents mass separation. In fact, the terms mass separation are not located within the specification and therefore Applicant’s amended claim language is not properly enabled by the specification” (see Office Action, page 3, lines 1-4).

In stating that the term “mass separation” is not located within the specification, the Office Action clearly errs. In fact, the term appears no less than five times within the specification.

For example, the specification states at page 11, lines 9-17, with emphasis added,

“B ions that are obtained by mass separation are implanted by ion implantation at a concentration of from  $1 \times 10^{16}$  to  $1 \times 10^{19} /cm^3$ . This method enables selective addition of B ions alone, and is therefore advantageous in controlling the quantity of addition (addition concentration). Plasma doping can be mentioned as an alternative method for ion implantation, but without using mass separation. In case such a means is used, a diffusion step must be incorporated because B ions are added as clusters together with other atoms and molecules.”

A similar discussion in another context provides another example (see specification, page 33, lines 10-17).

As another example, the specification states at page 21, lines 1-12, with emphasis added,

“In Example 1, the channel doping step is performed immediately after the formation of an island-like semiconductor layer. However, the channel-doping step can be effected between other steps. For instance, doping can be carried out on an amorphous silicon film before it is crystallized, or on a crystalline silicon film before it is patterned into an island-like semiconductor layer. In case of performing doping on an amorphous silicon film, in particular, ion implantation method without using mass separation (in which the ions to be added are implanted in the form of clusters) can be performed without any problem because the doped ions are allowed to diffuse uniformly into the film during the crystallization.”

As is clear from the above sections, and from various other discussions within the specification, there are various techniques for introducing an ion, such as a p-type ion including Boron, into a substance. For example, techniques such as ion implantation or plasma doping may be used.

When performing such implantation or doping, and considering Boron in particular, Boron, like many other elements, may not occur naturally in a convenient elemental form. Often a Boron-containing substance must be purified to some extent to obtain (substantially) pure Boron, such as by performing mass separation to avoid obtaining Boron atoms as part of "clusters together with other atoms and molecules" that have different masses (see specification, page 11, lines 16-17).

Typically, processes involving Boron-containing substances (e.g., without having had a mass separation performed) may be easier or cheaper to implement, since fewer process steps may be required. However, pure Boron and various Boron-containing substances may diffuse or otherwise behave differently from one another, depending on their individual properties and make-up.

As explained in the specification and discussed in more detail below, the method(s) recited in independent claim 1 advantageously allow the convenient introduction of ions without requiring mass separation. For example, independent claim 1 recites "introducing ions of a p-type impurity ... without mass separation," (e.g., using ion implantation or plasma doping), while independent claim 55, which Applicant believes to have been inadvertently withdrawn, recites "introducing ions of a p-type impurity ... by plasma doping without mass separation."

Based on the above, Applicant respectfully submits that the rejection under 35 USC 112 (1) is improper, and should be withdrawn. As a result, Applicant respectfully requests that the finality of the pending Office Action is improper, and also should be withdrawn. Further, inasmuch as no substantive rejection of (amended) claims 1, 2, 6, 7, 12-16, 38, and 46 (as well as claims 55-63, which Applicant believes to have been inadvertently withdrawn) has been issued, Applicant respectfully submits that all of these claims should now be passed to allowance.

Regarding new claims 64-68, Applicant also believes these claims to be in condition for allowance, and such action is requested. For example, claim 64 recites,

forming a layer of a crystalline semiconductor film on a surface of a substrate, where the layer includes a portion to be used as a channel region of a thin film transistor;

introducing ions of a p-type impurity into the portion;

selecting a temperature corresponding to a mobility of the ions with respect to an interface between the crystalline semiconductor film and an oxide;

subjecting the layer to a thermal oxidation process at the temperature to form a thermal oxide on the layer into which a portion of the ions diffuse from the crystalline semiconductor film, such that a desired concentration gradient of the ions within the crystalline semiconductor film is obtained that provides a corresponding adjustment to a threshold voltage of the thin film transistor.

Support for this claim is proved throughout the specification, including, for example, at page 12, line 6 to page 14, line 19. Specifically, as shown in FIGS. 4 and 5A, Boron has a diffusion coefficient that varies with temperature. Thus, by performing thermal oxidation at a particular temperature, the diffusion of (in this case) Boron may be finely controlled, so that an amount of Boron that diffuses out of a silicon layer and into an adjoining silicon oxide layer may be controlled. Thus, the Boron remaining in the silicon layer (i.e., in the channel region of a transistor) may be controlled so as to demonstrate a desired effect on the threshold voltage of the transistor.

In contrast, for example, Yamazaki '563 merely illustrates a doping/thermal oxidation process for a transistor (e.g., see FIG. 21C), in which some residual diffusion of previously-doped Boron may occur during a subsequent oxidation process. However, there is no disclosure or suggestion in Yamazaki '563 of "selecting a temperature corresponding to a mobility of the ions with respect to an interface between the crystalline semiconductor film and an oxide," as recited in new claim 64.

Moreover, there is no disclosure or suggestion in Yamazaki '563 of obtaining "a desired concentration gradient of the ions within the crystalline semiconductor film ... that provides a corresponding adjustment to a threshold voltage of the thin film transistor," as also recited in claim 64.

In this regard, it should be noted that Yamazaki does not appear to provide any teaching regarding an adjustment to a threshold voltage. For example, the August 14 Office Action points to the Abstract and column 21, lines 40-50 of Yamazaki '563 for this teaching. However, these sections deal only with a current leakage problem that results at sub-threshold levels.

That is, particular source/drain voltages imposed on a transistor may allow a drain current to flow even during a sub-threshold condition, as shown in FIG. 3. Yamazaki '563 proposes various solutions to this problem, including, for example, increasing a resistance within a channel region. In any case, modifying a threshold voltage of the transistor does not address this issue, and is not discussed in this context in Yamazaki.

Based on the above, Applicant respectfully submits that new claims 64-68 are allowable, and such action is hereby requested.